DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 15 February 2008. Applicant's arguments have been carefully and fully considered and are persuasive.

Claim Status

Claims 1-5, 7, 9, and 15 remain pending and are ready for examination.

Allowable Subject Matter

Claims 1-5, 7, 9, and 15 are allowed.

The following is an Examiner's statement of reasons for allowance: the prior art made of record fails to teach the combination including the limitation of:

(Claim **1**) "…when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal data transfer using the bus bridge function, the non-volatile memory having an area in which is stored information for indicating whether or not the data transfer control program information has been written correctly into the rewrite area.";

(Claim **7**) "…when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal

data transfer using the bus bridge function, the non-volatile memory having an area in which is stored rewriter processing setting information for setting whether processing by the rewriter is enabled or disabled; and the rewriter processing setting information being set to be enabled in an initial state but being set to be disabled at the end of processing by the rewriter.";

(Claim **9**) "…when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal data transfer using the bus bridge function, the non-volatile memory having an area in which is stored information for indicating whether or not the data transfer control program information has been written correctly into the rewrite area.";

(Claim **15**) "…when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal data transfer using the bus bridge information, the non-volatile memory having an area in which is stored rewriter processing setting information for setting whether processing by the rewriter is enabled or disabled; and the rewriter processing setting information being set to be enabled in an initial state but being set to be disabled at the end of processing by the rewriter."

As dependent claims **2-5** depend from an allowable base claim; they are at least allowable for the same reasons as noted *supra*.

The prior art made of record, neither anticipates nor renders obvious the above-recited combinations for at least the reasons specified and as shown in Applicant's Arguments filed 13 June 2007.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed 15 February 2008 have been carefully and fully considered, and are persuasive. As noted *supra* the case is in condition for allowance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLE/mb

/Kevin L Ellis/
Acting SPE of Art Unit 2187